

Semester- I

ADVANCED MACHINE LEARNING AND DEEP LEARNING			
Course Code	MEC101	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: - To understand the fundamental concepts of machine learning and its applications - To master the concepts of classification and clustering techniques. - To develop a deep understanding of convolutional neural networks (CNNs) and their architecture. - To apply deep learning techniques to large-scale datasets and real-world problems.			
Module-1			
Introduction to Machine Learning: Introduction, Training, Rote Learning, Learning Concepts, General-to-Specific Ordering, Version Spaces, Candidate Elimination, Inductive Bias, Decision-Tree Induction, The Problem of Overfitting, The Nearest Neighbor Algorithm, Learning Neural Networks, Supervised Learning, Unsupervised Learning, Reinforcement Learning.			
RBT Levels: L2, L3			
Module-2			
Neural Networks: Introduction, Neurons, Perceptrons, Multilayer Neural Networks, Recurrent Networks, Unsupervised Learning Networks, Evolving Neural Networks.			
RBT Levels: L3			
Module-3			
Convolutional Neural Networks: The operation, Pooling, Convolution and Pooling as an infinitely strong prior, Variants of the basic functions, efficient algorithms, Random or Unsupervised Features, Neuroscientific Basis for Convolutional Networks.			
RBT Levels: L3			
Module-4			
Recurrent Neural Networks: RNN, Bidirectional RNN, Encoder-Decoder Sequence to sequence architecture, Deep Recurrent Networks, Recursive Neural Networks, The Long Short Term Memory and other Gated RNNs, Optimization for Long Term Dependencies.			
RBT Levels: L3			
Module-5			
Applications: Large-Scale Deep Learning, Computer Vision, Speech Recognition, Natural Language Processing, Other Applications.			
RBT Levels: L3, L4			
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.			
Continuous Internal Evaluation: - Two Unit Tests each of 25 Marks - Two assignments each of 25 Marks or one Skill Development Activity of 50 marks to attain the COs and POs The sum of two tests, two assignments/skill Development Activities, will be scaled down to 50 marks CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.			
Semester-End Examination: - The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50. - The question paper will have ten full questions carrying equal marks. - Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.			

4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. Artificial Intelligence Illuminated - Ben Coppin
2. Deep Learning - Ian Goodfellow, Yoshua Bengio, Aaron Courville
3. Fundamentals of Deep Learning – Nikhil Budama
4. Neural Networks and Deep Learning – Charu Aggarwal
5. Hands-on Deep Learning Algorithms with Python – Sudharsan Ravichandran

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Skill Development Activities Suggested

- Individual or group projects to apply learned concepts to real-world problems.
- Regular coding assignments to reinforce theoretical concepts.
- Experimentation with different libraries and frameworks (e.g., TensorFlow, PyTorch, Scikit-learn).
- Guest lectures from industry experts to provide insights into current trends.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
C01	Demonstrate a comprehensive understanding of machine learning and deep learning fundamentals and their applications.	L2
C02	Apply various machine learning algorithms and deep learning architectures to solve complex problems.	L3
C03	Develop and implement machine learning models using appropriate programming languages and tools.	L4

Semester- I

ADVANCED EMBEDDED SYSTEMS			
Course Code	MEC102	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory +10 hours Lab	Total Marks	100
Credits	04	Exam Hours	03
Course Learning Objectives: - To understand the difference between Embedded Systems and General Computing Systems - To understand the Classification of Embedded Systems based on Performance, Complexity along with the Domains and Areas of Applications of Embedded Systems - Analysis of a Real Life example on the bonding of Embedded Technology with Human Life - To understand the difference between Microcontrollers and ARM Cortex processors. - To learn Programming using assembly and C language, CMSIS for variety of End Applications.			
Module - 1			
Embedded System: Embedded v/s General Computing System, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems. RBT Levels: L2, L3			
Module - 2			
Hardware Software Co-Design: Embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging. RBT Levels: L3			
Module - 3			
ARM - 32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence. RBT Levels: L3			
Module - 4			
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface, Exceptions, Nested Vector interrupt controller design, SysTick Timer, Cortex- M3 Programming using assembly and C language, CMSIS. RBT Levels: L3			
Module - 5			
Introduction to RISC - V: Operations of the Computer Hardware, Operands of the Computer Hardware, Signed and Unsigned Numbers, Representing Instructions in the Computer, Logical Operations, Instructions for Making Decisions, RISC-V Addressing for Wide Immediate and Addresses, Parallelism and Instructions: Synchronization RBT Levels: L3, L4			

PRACTICAL COMPONENT OF IPCC Using suitable simulation software in Linux Develop and test Assembly Language Program (ALP) using ARM/RISC Processor.	
1.	Develop and test programs: a) To create child process and display it's ID. b) Execute child process function using switch structure.
2.	Develop and test the program for a multi-threaded application, where communication is through shared memory for the conversion of lowercase text touppercase text.
3.	Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosen application.
4.	Create 'n' number of child threads. Each thread prints the message "I'm in thread number ..." and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.
5.	Implement the multi-thread application satisfying the following: a) Two child threads are created with normal priority. b) Thread 1 receives and prints its priority and sleeps for 50ms and then quits. c) Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits. d) The main thread waits for the child thread to complete its job and quits.
6.	Write ALP to find the square of a number (1 to 10) using look-up table.
7.	Write an ALP to arrange a series of 32 bit numbers in ascending/descending order.
8.	Write an ALP to count the number of ones and zeros in two consecutive memory locations.
9.	Interface a simple Switch and display its status through Relay, Buzzer and LED. (Study Expt.)
10.	Implement a clock capable of displaying (and being set to the correct time). Include an alarm facility which can be set by the user and will 'go off' at the correct time.

Assessment Details (both CIE and SEE): The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester EndExam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. CIE for the theory component of IPCC - Two Tests each of 20 Marks - Two assignments each of 10 Marks / One Skill Development Activity of 20 Marks - Total Marks of two tests and two assignments / One Skill Development Activity added will be CIE for 60 Marks, marks scored will be proportionally scaled down to 30 Marks. CIE for the practical component of IPCC - On completion of every experiment / program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The 15 Marks are for conducting the experiment and preparation of the laboratory record, the other 05 Marks shall be for the test conducted at the end of the semester. - The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks. - The laboratory test at the end /after completion of all the experiments shall be conducted for 50 Marks and scaled down to 05 Marks. Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for 20 marks. SEE for IPCC Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours) - The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks. - The question paper will have ten questions. Each question is set for 20 marks. - There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), should have a mix of topics under that module. - The students have to answer 5 full questions, selecting one full question from each module. The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component. - The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks -30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

2. SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course (CIE+SEE))

Suggested Learning Resources:

Text Books

1. 'Introduction to embedded systems', K. V. Shibu, TMH education Pvt. Ltd., 2009.
2. 'The Definitive Guide to the ARM Cortex-M3', Joseph Yiu, Newnes, (Elsevier), 2nd edn, 2010.
3. 'Computer Organization and Design RISC-V Edition', David A. Patterson, John L. Hennessy, Morgan Kaufmann, ISBN: 9780128122761.

Reference Books

1. 'Embedded systems - A contemporary design tool', James K. Peckol, John Wiley, 2008

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in/>

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research / testing / projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No	Course Outcomes	Blooms Level
CO 1	Understand the basic hardware components and their selection methods based on the attributes of Embedded Systems	L2
CO 2	Describe the code design process and firmware design approaches	L2
CO 3	Acquaint the knowledge of ARM Cortex M3 Processor and its salient features.	L3
CO 4	Understand the basics of RISC - V Architecture.	L3
CO 5	Apply and use Programming Techniques for different End Uses	L3, L4

Semester- I

DIGITAL CIRCUITS & LOGIC DESIGN			
Course Code	MEC103	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: • Understand the concepts of sequential machines • Design Sequential Machines/Circuits • Analyze the faults in the design of circuits • Apply fault detection experiments to sequential circuits			
Module-1			
Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.			
RBT Levels: L2, L3			
Module-2			
Fault detection by path sensitizing: Detection of multiple faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.			
RBT Levels: L3			
Module-3			
Fault-location experiments: Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.			
RBT Levels: L3			
Module-4			
Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, decompositions, Synthesis of Multiple Machines.			
RBT Levels: L3			
Module-5			
State Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.			
RBT Levels: L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:**Textbook:**

1. 'Switching and Finite Automata Theory', Zvi Kohavi, TMH, ISBN: 978_0_07_099387_7, 2nd Edition, 2008.

Reference Books:

1. 'Digital Circuits and logic Design', Charles Roth Jr., Cengage Learning, 7th edition, 2014.
2. 'Fault Tolerant and Fault Testable Hardware Design', Parag K Lala, Prentice Hall Inc. 1985.
3. 'Introductory Theory of Computer', E. V. Krishnamurthy, Macmillan Press Ltd, 1983
4. 'Theory of computer science – Automata, Languages and Computation', Mishra & Chandrasekaran, 2nd Edition, PHI, 2004.

Web links and Video Lectures (e-Resources):

<https://nptel.ac.in/>

Skill development activities: Under Skill development activities in a concerning course, the students should

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

CO	Description	Blooms Level
CO1	Able to understand the concepts of sequential machines.	L2
CO2	Able to understand the Sequential Machines/Circuits.	L2
CO3	Able to understand the structure of sequential machines.	L2
CO4	Able to analyse the faults in the design of circuits.	L3, L4
CO5	Able to analyse fault detection experiments to sequential circuits.	L3, L4

Semester- I

ASIC DESIGN			
Course Code	MEC114A	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Course Learning objectives: • To learn ASIC methodologies and programmable logic cells to implement a function on IC. • To Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing. • To Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs			
Module-1			
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. CMOS Logic: Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carryselect, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.			
RBT Levels: L2			
Module-2			
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi-stage cells, Optimum delay and number of stages, library cell design.			
Programmable ASIC Logic Cells: MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA:XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block			
RBT Levels: L2, L3			
Module-3			
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.			
ASIC Construction: Physical Design, CAD Tools System partitioning, Estimating ASIC size. Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.			
RBT Levels: L2, L3			
Module-4			
Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.			
Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.			
RBT Levels: L2, L3			
Module-5			
Routing: Global Routing - Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing - Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.			
RBT Levels: L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:**Books**

1. Michael John Sebastian Smith, "Application - Specific Integrated Circuits", Addison- Wesley Professional, 2005
2. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison Wesley/ Pearson education 3rd edition, 2011
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations" Springer, ISBN: 978-1-4614-1119-2. 2011
4. Rakesh Chadha, Bhasker J, "An ASIC Low Power Primer", Springer, ISBN: 978-14614-4270-7.
5. Peter J. Ashenden Digital Design (Verilog): An Embedded Systems Approach Using Verilog, 1st Edition, Kindle Edition.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Skill Development Activities Suggested

- Activity Based Learning (Suggested Activities in Class)/ Practical Based learning
- Real world Problem Solving: Applying the ASIC front end and backend concepts.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Describe the concepts of ASIC design methodology, data path elements, logical effort.	L2
CO2	Analyze the design of ASICs suitable for specific tasks, perform design entry and explain the physical design flow.	L3
CO3	Design data path elements for ASIC cell libraries and compute optimum path delay.	L3
CO4	Create floor plan including partition and routing with the use of CAD algorithms	L3,L4
CO5	Design CAD algorithms and explain how these concepts interact in ASIC design.	L3,L4

Semester 1

ADVANCED COMPUTER NETWORKING			
Course Code	MEC114B	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
Course Learning objectives: This Course will enable students to • Focus on advanced networking concepts for next generation network architecture and design. • Acquire knowledge about SDN and virtualization for designing next generation networks.			
Module-1			
Medium Access Control Sub Layer: Wireless LANs, Broadband Wireless, Bluetooth, RFID. The Network Layer: Network Layer Design Issues, Congestion Control Algorithms, Quality of Service, The Network Layer in the Internet.			
RBT Levels: L2			
Module-2			
The Application Layer: The Domain Name System, Electronic Mail, The World Wide Web.			
RBT Levels: L2, L3			
Module-3			
Software Defined Network (SDN): Evolution of Switches and Control Planes, Cost, SDN Implications for Research and Innovation Genesis of SDN: The Evolution of Networking Technology, Forerunners of SDN, Software Defined Networking is Born, Sustaining SDN Interoperability, Open Source Contributions, Network Virtualization How SDN Works: Fundamental Characteristics of SDN, SDN Operation, SDN Devices, SDN Controller, SDN Applications, Alternate SDN Methods			
RBT Levels: L2, L3			
Module-4			
The Openflow Specification: OpenFlow Overview, OpenFlow 1.0 and OpenFlow Basics, OpenFlow Additions - 1.1, 1.2, 1.3, 1.4, 1.5, Improving OpenFlow Interoperability, Optical Transport Protocol Extensions, OpenFlow Limitations			
RBT Levels: L2, L3			
Module-5			
Network Functions Virtualization: Definition of NFV, Virtualize, Standards, OPNFV, Leading NFV Vendors, SDN Vs NFV, In-Line Network Functions. SDN Open Source: SDN Open Source Landscape, The OpenFlow Open Source Environment, Profiles of SDN Open Source Users, OpenFlow Source Code, Switch Implementations, Controller Implementations, SDN Applications, Orchestration and Network Virtualization, Simulation, Testing and Tools, Open Source Cloud Software, Example: Applying SDN Open Source.			
RBT Levels: L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:**Text Books:**

1. Andrew S. Tanenbaum, David J. Wetherall, Computer Network, 5th Edition. Pearson Education.
2. Paul Goransson, Chuck Black and Timothy Culver, Software Defined Networks – A Comprehensive Approach, 2nd Edition, 2017, Morgan Kaufmann.

Reference books:

1. Behrouz A. Forouzan, Data Communications and Networking, Fourth Edition, Tata McGraw Hill, 2007.
2. James F Kurose, Keith W Ross, Computer Networking- A Top-down Approach Featuring the Internet, 7th Edition, 2017, Pearson Education.
3. Alberto Leon Garcia, Indra Widjaja, Communication Networks-Fundamental Concepts and Key Architectures, Fifth reprint 2002 , Tata McGraw Hill.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Skill Development Activities Suggested

- The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
CO1	Understand advanced concepts and next generation networks.	L2
CO2	Analyze network Algorithms, Protocols and their functionalities.	L3
CO3	Comprehend features of SDN and its application to next generation systems.	L3
CO4	Analyze the performance of various server implementations.	L3, L4

Semester- 1

ADVANCED SIGNAL PROCESSING			
Course Code	MEC114C	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: - To know the analysis of discrete time signals. - To study the modern digital signal processing algorithms and applications. - To Have an in-depth knowledge of use of digital systems in real time applications - To apply the algorithms for wide area of recent applications.			
Module-1			
Analysis of Discrete Time Signals: Basic elements of a DSP System – Review of Sampling and Quantisation – Sampling theorem for low pass and band pass signals, uniform and non-uniform quantization, Application of quantisation in lossy compression of signals – Lloyd Max quantizer; Fourier analysis of Continuous and Discrete time signals –Review of Fourier series and Fourier transform, Discrete Time Fourier Transform (DTFT), Discrete Fourier Transform (DFT), Interpretation of DFT Spectrum, Review of DFT properties – Convolution and correlation, Convolution of long sequences, Leakage effect, Windowing – Introduction to other transforms : Discrete Cosine Transform (DCT), Walsh Hadamard Transform (WHT), Karhunen Loeve Transform (KLT) – Applications.			
RBT Levels: L2, L3			
Module-2			
Digital Filters and Implementation: Review of FIR and IIR filter design – Notch filter– Comb filter– All pass filters – Applications – Structures for digital filter realization: Signal flow graph and block diagram representations, FIR and IIR Filter structures, Lattice structures – Finite word length effects – Fixed-point and floating-point DSP arithmetic, Effects of quantization, Scaling, Limit cycles in fixed point realizations of IIR digital filters, Limit cycles due to overflow. Quantization effect in DFT and FFT computation.			
RBT Levels: L3, L4			
Module-3			
Multirate Signals and Systems: Introduction to multirate signal processing with applications, Multirate System Fundamentals – Decimation and Interpolation, Transform domain analysis of Decimators and Interpolators, Decimation and Interpolation filters, Fractional sampling rate alteration, Practical sampling rate converter design.			
RBT Levels: L3, L4			
Module-4			
Introduction to 2-D Signals and Systems: Polyphase decomposition and efficient structures – Introduction to digital filter banks – The DFT filter bank, Two Channel Quadrature Mirror Filter bank (QMF), Perfect Reconstruction.			
RBT Levels: L3, L4			
Module-5			
Introduction to 2-D Signals and Systems: Elementary 2D signals – Linear shift Invariant systems – Separability – 2D convolution – Introduction to 2D transforms: 2D DFT, 2D DCT, Applications.			
RBT Levels: L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:**Books**

1. John G. Proakis, Dimitris G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 4th Edition, Pearson India, 2007.
2. P.P. Vaidyanathan, Multirate systems and filter banks, 2nd Edition, Pearson Education India, 1992.
3. Lim J. S., Two-dimensional signal and image processing, Prentice Hall, 1990.
4. K Deergha Rao, M N S Swamy, Digital Signal Processing: Theory and Practice, Springer, 2018.
5. Steven W. Smith, The Scientist and Engineer's Guide to Digital Signal Processing, California, 1999.
6. Mitra S. K., Digital Signal Processing: A Computer Based Approach, McGraw-Hill Publishing Company, 2013

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Skill Development Activities Suggested

- Mini Project in the area Advanced signal processing using modern tools like MATLAB, Python etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyze the effect of sampling and quantisation of signals and appraise its relevance with reference to applications.	L2, L3
CO2	Formulate various transform domain representations of 1D and 2D signals and demonstrate their applications with reference to practical signals.	L3, L4
CO3	Examine finite word length effects and design practical filters for real life.	L3, L4
CO4	Demonstrate the effect of sampling rate converters and design distortion free digital filter banks illustrating their applications to process real life signals.	L3, L4
CO5	Analyze and choose architectures to efficiently implement the DSP systems for various applications taking into consideration the practical aspects.	L3, L4

Semester- 1

POWER CONVERTERS			
Course Code	MEC114D	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: • To analyse switched circuits. • To analyse single phase and three phase AC to DC converters. • To analyse and design DC to DC converters. • To analyse DC to AC converters. • To analyse AC to AC converters.			
Module-1			
Analysis of switched circuits: thyristor controlled half wave rectifier – R, L, RL, RC load circuits, classification and analysis of commutation.			
RBT Levels: L3			
Module-2			
Single-Phase and Three-Phase AC to DC converters: half controlled configurations- operating domains of three phase full converters and semi-converters – Reactive power considerations.			
RBT Levels: L3			
Module-3			
Analysis and design of DC to DC converters: Control of DC-DC converters, Buck converters, Boost converters, Buck-Boost converters, Cuk converters.			
RBT Levels: L3, L4			
Module-4			
Single phase and Three phase inverters: Voltage source and Current source inverters, Voltage control and harmonic minimization in inverters.			
RBT Levels: L3			
Module-5			
AC to AC power conversion using voltage regulators: choppers and cyclo-converters, consideration of harmonics.			
RBT Levels: L3			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:**Books**

1. Ned Mohan, Undeland and Robbin, 'Power Electronics: converters, Application and design', John Wiley and sons.Inc, Newyork, 1995.
2. Rashid M.H., 'Power Electronics Circuits, Devices and Applications ', Prentice Hall India, New Delhi, 1995.
3. P.C Sen., 'Modern Power Electronics ', Wheeler publishing Co, First Edition, New Delhi, 1998.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyse switched circuits.	L3
CO2	Analyse single phase and three phase AC to DC converters.	L3
CO3	Analyse and design DC to DC converters.	L3, L4
CO4	Analyse DC to AC converters.	L3
CO5	Analyse ACto AC converters.	L3

Semester- 1

SYSTEMVERILOG			
Course Code	MEC115A	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: This course will enable students to: • Understand Digital System Verification Using Object Oriented Methods • Learn the System Verilog Language for Digital System Verification. • Create/Build Test Benches for the Design/Methodology. • Use Constrained Random Tests for Verification • Understand Concepts of Functional Coverage			
Module-1			
Verification Guidelines: The Verification Process, Basic Test Bench Functionality, Directed Testing, Methodology Basics, Constrained Random Stimulus, Randomization, Functional Coverage, Test Bench Components, Layered Test Bench. Data Types: Built-In Data Types, Fixed and Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, Choosing A Storage Type, Creating New Types With typedef, Creating User Defined Structures, Type Conversion, EnumeratedTypes, Constants and Strings, Expression Width.			
RBT Levels: L2, L3			
Module-2			
Procedural Statements and Routines: Procedural Statements, Tasks, Functions and Void Functions, Task and Function Overview, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values. Connecting the Test Bench and Design: Separating the Test Bench and Design, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, System Verilog Assertions.			
RBT Levels: L2, L3			
Module-3			
Randomization: Introduction, Randomization in System Verilog, Constraint Details, Solution Probabilities, Valid Constraints, InLine Constraints, Random Number Functions, Common Randomization Problems, Random Control, Random Number Generators.			
RBT Levels: L3			
Module-4			
Threads and Inter process Communication: Working with Threads, Disabling Threads, Inter Process Communication, Events, Semaphores, Mailboxes, BuildingA Test Bench with Threads and InterProcess Communication.			
RBT Levels: L3			
Module-5			
Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Anatomy of Cover Group, Triggeringa CoverGroup, Data Sampling, Cross Coverage, Generic Cover Groups, Coverage Options, Analyzing Coverage Data, MeasuringCoverage Statistics During Simulation.			
RBT Levels: L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:**Books**

1. Chris Spear, "System Verilog for Verification – A guide to learning the Test bench language features", Springer Publications Second Edition, 2010.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design- A guide to using system Verilog for Hardware design and modelling", Springer Publications Second Edition, 2006.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Skill Development Activities Suggested:

- 1) Interact with industry (small, medium, and large).
- 2) Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
- 3) Involve in case studies and field visits/ fieldwork.
- 4) Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
- 5) Handle advanced instruments to enhance technical talent.
- 6) Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
- 7) Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Apply the SystemVerilog concepts to verify the design.	L3
CO2	Apply constrained random tests benches using SystemVerilog.	L3
CO3	Appreciate Functional Coverage.	L3, L4

Semester-I

ADVANCED WIRELESS COMMUNICATION			
Course Code	MEC115B	CIE Marks	50
Teaching Hours/Week(L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3
Course Learning objectives: 1. To enable students understand the various aspects of wireless communication 2. To understand the concept behind the capacity of channels. 3. Gain the information on Linear time-invariant Gaussian channels, Capacity of fading channels 4. Study uplink and downlink model of AWGN channel, fading channels 5. Describe different types of diversity, Understanding concept behind modeling of MIMO.			
Module-1			
Physical modeling for wireless channels, Input/output model of the wireless channel: Free space, fixed transmit and receive antennas, Free space, moving antenna, Reflecting wall, fixed antenna, Reflecting wall, moving antenna, Reflection from a ground plane, Power decay with distance and shadowing, Moving antenna, multiple reflectors, The wireless channel as a linear time-varying system, Baseband equivalent model, discrete-time baseband model, Additive white noise.			
RBT Levels: L2			
Module-2			
Time and frequency coherence, AWGN channel capacity: Time and frequency coherence: Doppler spread and coherence time, delay spread and coherence bandwidth, Repetition coding, Packing spheres, Capacity-achieving AWGN channel codes, Reliable rate of communication and capacity, Resources of the AWGN channel-Continuous-time AWGN channel, Power and bandwidth, Bandwidth reuse in cellular systems.			
RBT Levels: L2, L3			
Module-3			
Linear time-invariant Gaussian channels, Capacity of fading channels: Single input multiple output (SIMO) channel, Multiple input single output (MISO) channel, Frequency-selective channel, Slow fading channel, receive diversity, Transmit diversity, Transmit and receive diversity, Time and frequency diversity, Outage for parallel channels, Fast fading channel, Transmitter side information, Frequency-selective fading channels.			
RBT Levels: L2, L3			
Module-4			
Uplink and Downlink AWGN channel, Uplink and Downlink fading channel: Capacity via successive interference cancellation, Comparison with conventional CDMA, Comparison with orthogonal multiple access, General K-user uplink capacity, Symmetric case: two capacity achieving schemes, General case: superposition coding achieves capacity, Slow fading channel, Fast fading channel, Full channel side information, Channel side information at receiver only, Full channel side information, Frequency selective fading channels.			
RBT Levels: L2, L3			
Module-5			
Multiuser diversity, Physical Modeling of MIMO channels: Multiuser diversity gain, Multiuser versus classical diversity, Fair scheduling and multiuser diversity, Channel prediction and feedback, Opportunistic beam forming using dumb antennas, Multiuser diversity in multicell systems, Line-of-sight SIMO channel, Line-of-sight MISO channel, Antenna arrays with only a line-of-sight path, Geographically separated antennas, Line-of-sight plus one reflected path, MIMO multipath channel, Angular domain representation of signals, Angular domain representation of MIMO channels, Statistical modeling in the angular domain, Degrees of freedom and diversity, Dependency on antenna spacing.			
RBT Levels: L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**.
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the Cos and Pos.

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks CIE methods/question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:**Books**

1. Andrea Goldsmith, Wireless Communications, Cambridge University Press, 2005.
2. David T, Pramod Viswanath, Fundamentals of Wireless Communications, Cambridge.

Weblinks and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
C01	Implement physical models of wireless channels. Gain knowledge on communication links and physical model.	L3, L4
C02	Gain knowledge of key concepts of wireless communication	L3
C03	Measure capacity of AWGN channel, LTI Gaussian channels and various fading channels.	L3
C04	Study uplink and downlink model of AWGN channel, fading channels and multiuser diversity.	L2, L3

MULTIMEDIA AND APPLICATIONS			
Course Code	MEC115C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Course objectives: This course will enable students to: - Understanding basics of multimedia including text, image, audio, video and multimedia networking terminology. - Explore how multimedia is used in different applications like image compression and text compression. - Understand various audio and video compression techniques. - Comprehend the various video compression standards and Multimedia Networks with applications.			
Module-1			
Introduction: Multimedia information representation, Multimedia networks, Multimedia applications, Application and networking terminology, Network QoS and application QoS, Digitization principles, Text, images, audio and video.			
RBT Levels: L2			
Module-2			
Text and image compression: Compression principles, Text compression- Run length, Huffman, LZW, Document Image compression using T2 and T3 coding, image compression- GIF, TIFF and JPEG.			
RBT Levels: L3			
Module-3			
Audio and Video Compression: Audio compression – principles, DPCM, ADPCM, Adaptive and Linear Predictive coding, Code-Excited LPC, Perceptual coding, MPEG and Dolby coders video compression, Video compression principles.			
RBT Levels: L3			
Module-4			
Video Compression Standards: H.261, H.263, MPEG, MPEG 1, MPEG 2, MPEG-4 and Reversible VLCs, MPEG-7 standardization process of multimedia content description, MPEG 21 multimedia framework.			
RBT Levels: L3			
Module-5			
Multimedia Networks: Basics of Multimedia Networks, Communications and Applications: Quality of Multimedia Data Transmission, Multimedia over IP, Multimedia over ATM Networks, Transport of MPEG-4, Media on Demand (MoD).			
RBT Levels: L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks**

to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:**Text Books:**

1. Fred Halsall, "Multimedia Communications: Applications, Networks, Protocols and Standards" Pearson Education Publishers, 2001, ISBN: 97802013981871.
2. Raif Steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002.

Reference Books:

1. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004.
2. Hans. W. Barz, Gregory A. Bassett, "Multimedia Networks: Protocols, Design and Applications", John Wiley & Sons publications, 2016. ISBN: 9781119090137.
3. John Billamil, Louis Molina, "Multimedia: An Introduction", PHI, 2002.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Semester Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
C01	Deploy the right multimedia communication models.	L3, L4
C02	Apply QoS to multimedia network applications with efficient routing techniques.	L3
C03	Discuss the various standards and quality aspects of digital video formats used for multimedia application.	L2
C04	Solve the security threats in the multimedia networks.	L3
C05	Develop the real-time multimedia network applications.	L4

Semester- I

PROCESS CONTROL			
Course Code	MEC115D	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: - To understand the need of process control, basic principles of various manufacturing processes and apply engineering knowledge to do problem analysis in process control. - To define common dynamics of processes found in many industries and model them mathematically. - To select the proper controller and apply the tuning rules to achieve optimum performance. - To understand, interpret and implement tuning of the controllers using various methods and study about digital controllers. - To select advanced control strategy to enhance the performance.			
Module-1			
Introduction: Introduction to Process Control. Control objectives, servo regulatory control, and classification of process variables. Modeling of some Chemical Process Systems: Modeling basics, Degree of Freedom, Mass Balance, Energy Balance equations, linearization of nonlinear systems, Modeling of Level Tank System, Continuous Stirred Tank Heater, Continuous Stirred Tank Reactor, Transfer function.			
RBT Levels: L2			
Module-2			
Elements of Process Control: Dead time, Interacting and non-interacting systems, self-regulation, inverse response, capacity of process, integrating systems, multi-capacity process. Process Identification: Dynamic behavior of first and second order processes, Obtaining First Order Plus Time Delay (FOPTD) model with Process Reaction curve. Obtaining second order model of processes.			
RBT Levels: L2, L3			
Module-3			
Common Controller Modes: Controller Modes, ON OFF, Multi position, time proportional controller, Theory Proportional, Integral and Derivative modes, PI, PD, PID Controller, Electronics Controller implementation, Dynamic Behavior of closed loop systems with P, I, D, PI, PID modes.			
RBT Levels: L2, L3			
Module-4			
Discretisation and Implementation Issues: Discrete time control mode realization. Velocity and Position algorithm of PID control. Integral windup, anti-windup systems, controller bias, bumps less transfer. Tuning of Controllers: Application and tuning, ZN Tuning (Open loop and Closed loop), Performance criteria, Integral criteria.			
RBT Levels: L3, L4			
Module-5			
Some Advance Control Techniques: Cascade Control, Feed forward Control, ratio Control, Air Fuel Ratio Control for Drum Boilers. Level Control in Drum Boiler, Shrinking and Swelling, Inverse response of Drum Boiler.			
RBT Levels:L3, L4			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.

Suggested Learning Resources:**Books**

1. G. Stephanopolous, "Chemical Process Control An Introduction to Theory and Practice", Prentice Hall India, August 2000.
2. Surekha Bhanot, "Process Control Principles and Applications", Oxford, 2008
3. C.D. Johnson, "Process Control Instrumentation Technology", Prentice Hall India.
4. Thomas Marlin, "Process Control Designing Processes and Control for Dynamic Performance", Tata MC Graw Hill, 2012.
5. F.G. Shinskey, "Process Control Systems Application Design and Adjustment" 3rd edition, McGraw Hill International, 6. D. E. Seborg, T.F. Edgar, D. A. Mellichamp, "Process Dynamics and Control", Wiley, 2004.

Web links and Video Lectures (e-Resources):

- <https://nptel.ac.in/>

Skill Development Activities Suggested

- To develop a simple control loop for a system using microcontroller or hardware circuit e.g. on off control of heaters/temperature control systems, displaying of the variables on computer screens or LCD screens etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Understand the need of process control, basic principles of various manufacturing processes and apply engineering knowledge to do problem analysis in process control.	L2, L3
CO2	Define common dynamics of processes found in many industries and model them mathematically.	L2
CO3	Select the proper controller and apply the tuning rules to achieve optimum performance.	L3
CO4	Understand, interpret and implement tuning of the controllers using various methods and study about digital controllers.	L2, L3, L4
CO5	Select advanced control strategy to enhance the performance.	L3

ADVANCED MACHINE LEARNING AND DEEP LEARNING LAB			
Course Code	MECL116A	CIE Marks	50
Teaching Hours/Week (L:P:T/SDA)	0:4:0	SEE Marks	50
Credits	02	Exam Hours	03
Course Objectives: - To apply theoretical knowledge to practical scenarios. - To gain proficiency in implementing machine learning algorithms. - To analyse real-world problems and develop appropriate solutions.			
Sl.No.	Experiments		
1	Implement multivariate linear regression.		
2	Implementing Decision tree Classification.		
3	Implement K-means clustering algorithm.		
4	Write a program for Gradient Descent Learning.		
5	Implement Bidirectional Recurrent neural network.		
6	Implementation of Natural Language Processing.		
7	Implementation of Speech Recognition.		
8	Case study- Convolutional Neural Networks.		
	Demonstration Experiments (For CIE)		
9	Visualizing linear regression: Use a physical model or software to demonstrate how a line fits to data points.		
10	Overfitting and underfitting: Demonstrate the effects of overfitting and underfitting using simple datasets.		
11	Convolution operation: Visualize the convolution process using image patches.		
12	Language modelling: Generate text using a simple RNN model.		
Course outcomes (Course Skill Set): At the end of the course the student will be able to: 1. Implement and apply machine learning techniques in prediction problems. 2. Implement suitable learning algorithms to solve a given problem. 3. Implement a model based on machine learning for an application.			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination(SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- **Total marks scored by the students are scaled down to 30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- **The test marks is scaled down to 20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and marks of test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Suggested Learning Resources:

- Deep Learning - Goodfellow, Bengio and Courville
- Fundamentals of Deep Learning – Nikhil Budama
- Neural Networks and Deep Learning – CharuAggarwal
- Hands-on Deep Learning Algorithms with Python – SudharsanRavichandran

ELECTRONICS AND COMMUNICATIONLABORATORY			
Course Code	MECL116B	CIE Marks	50
Teaching Hours/Week (L:P:T/SDA)	0:4:0	SEE Marks	50
Credits	02	Exam Hours	03
Course Objectives: • To apply theoretical knowledge to practical scenarios. • To design and analyseanalog and mixed-signal circuits. • To implement and evaluate timing and oscillation circuits. • To analyse and implement communication systems.			
Sl.No.	Experiments		
Part - A			
1	Design a Two-Stage direct coupled Differential Amplifier with series voltage Negative Feedback of $\beta=50$.		
2	Design a Voltage regulator using operational amplifier to produce output of 12V with maximum load current of 50mA.		
3	Design a Two-stage CS Amplifier with overall gain of 100. Plot the frequency response and estimate the Bandwidth and Q factor.		
4	Design a Darlington Emitter follower using MOSFET/BJT with and without bootstrap; plot the frequency response. Also calculate gain and bandwidth.		
5	Design and realize:i) Four-bit weighted R – 2R ladder DAC. ii) Two-bit Flash ADC using Op-amp.		
6	Design and verify an IC 555 timer-based pulse generator for the specified pulse of 2ms.		
7	Using IC NE 566 Voltage Controlled Oscillator, design a circuit to generate square and triangular waveform with a time period of 0.2ms.		
Part - B			
8	Design a radio receiver for a given frequency (88 to 108 MHz) and measure the sensitivity, selectivity, and fidelity of the same.		
9	Generate PAM and PDM signals for a pulse duration of 10 msec using IC 555 Timer.		
10	Implement an AM and FM systems and measure its noise figure.		
11	Consider the bit sequence of length 10,000. Modulate it with BPSK, BASK, BFSK. Transmit the signal through AWGN channel. Vary the SNR. Compare the theoretical and simulated probability of error.		
12	Design and implement the Adaptive delta modulation and demodulation.		
Courseoutcomes(CourseSkillSet): At theendofthecourse thestudent will beableto: 1. Analyze frequency response of BJT/ MOSFET circuits. 2. Design Analog circuits using OPAMPs and IC555 for different applications. 3. Design and test circuits for Analog and digital modulation/demodulation schemes. 4. Design and test circuits for Analog to digital signal conversion techniques. 5. Design and analysis of feedback circuits.			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has to secure 50% maximum marks of the course.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- **Total marks scored by the students are scaled down to 30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 01 tests for 100 marks, test shall be conducted after the 14th week of the semester.
- In test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- **The test marks is scaled down to 20 marks** (40% of the maximum marks).

The Sum of **scaled-down** marks scored in the report write-up/journal and marks of test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours

Suggested Learning Resources:

- "Analog Integrated Circuit Design" by David A. Johns and Ken Martin.
- "Design of Analog CMOS Integrated Circuits" by Behzad Razavi.
- "Op-Amps and Linear Integrated Circuits" by Ramakant A. Gayakwad.
- "555 Timer IC: Operation and Application" by Michael T. R. R. Haskell.
- "Communication Systems" by Simon Haykin.
- "Digital Communications" by John G. Proakis and Masoud Salehi.

SEMESTER - II

ANTENNA THEORY AND DESIGN			
Course Code	MLEL201	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(3:2:0)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 10-12 Lab slots	Total Marks	100
Credits	4	Exam Hours	03
Course objectives: This course will enable students: • To classify different types of antennas • To define and illustrate various types of array antennas • To design antennas like Yagi-Uda, Helical antennas and other broadband antennas • To describe different antenna synthesis methods. • To apply methods like Method of Moments, Pocklington's integral equation, Source modeling.			
MODULE-1			
Antenna Fundamentals and Definitions: Radiation Mechanisms, Overview, EM Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation patterns, Directivity and Gain, Antenna impedance, Radiation efficiency, Antenna polarization. TEXT(1) RBT Levels: L2, L3			
MODULE-2			
Arrays: Array factor for linear arrays, Uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Nonuniformly excited equally spaced linear arrays, Mutual coupling. Antenna Synthesis: Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Fourier series, Woodward - Lawson sampling method, Comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array, Taylor line source method. TEXT(1) RBT Levels: L2, L3			
MODULE-3			
Resonant Antennas: Wires and Patches, Dipole antenna, Yagi-Uda antennas, Micro-strip antenna. Broadband antennas: Traveling wave antennas, Helical antennas, Biconical antennas, Sleeve antennas, and Principles of frequency independent antennas, Spiral antennas, and Log-periodic antennas. TEXT(1) RBT Levels: L2, L3			
MODULE-4			
Aperture antennas: Techniques for evaluating gain, Reflector antennas, Parabolic reflector antenna principles, Axis-symmetric parabolic reflector antenna, offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice. TEXT(1) RBT Levels: L2, L3			
MODULE 5			
Antenna in systems & Measurements: Receiving properties of antennas, Antenna temperature & radiometry. CEM for antennas: The method of moments: Introduction of the method moments, Pocklington's integral equation, Integral equation and Kirchhoff's network equations, Source modeling, weighted residual formulations and computational consideration, Calculation of antenna and scatter characteristics. TEXT(1). RBT Levels: L2, L3			

PRACTICAL COMPONENT OF IPCC: Conduct the experiments using MATLAB / Scilab / any antenna simulation tool

Sl.NO	Experiments
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1	MATLAB/Implementation to obtain the radiation pattern of an antenna
2	Study of radiation pattern of different antennas.
3	Determine the directivity and gain of Horn/ Yagi/dipole/ Parabolic antennas.
4	Impedance measurements of Horn antennas.
5	Study of radiation pattern of E-plane horns
6	Significance of Pocklington's integral equation.
7	Determine the directivity and gain of dipole antennas.
8	Impedance measurements of Yagi antennas.
9	Determine the directivity and gain of Parabolic antennas.
10	Study of radiation pattern of E-plane horns

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

1. Two Tests each of **25 Marks**
2. Two assignments each of **25 Marks/One Skill Development Activity of 50 marks**
3. Total Marks of two tests and two assignments/one Skill Development Activity added will be CIE for 60 marks, marks scored will be proportionally scaled down to **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for **10 marks**. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test at the end /after completion of all the experiments shall be conducted for **50 marks** and scaled down to **05 marks**.

Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

1. The question paper will be set for 100 marks and marks scored will be scaled down proportionately to 50 marks.
2. The question paper will have ten questions. Each question is set for 20 marks.
3. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
4. The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component).

- The minimum marks to be secured in CIE to appear for SEE shall be the 15 (50% of maximum marks-30) in the theory component and 10 (50% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included. The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.
- SEE will be conducted for 100 marks and students shall secure 40% of the maximum marks to qualify in the SEE. Marks secured will be scaled down to 50. (Student has to secure an aggregate of 50% of maximum marks of the course (CIE+SEE)

Suggested Learning Resources:

Textbook:

1. 'Antenna Theory and Design', Stutzman and Thiele, John Wiley, 2nd Edition, 2010

Reference Books:

1. 'Antenna Theory Analysis and Design', C.A. Balanis, John Wiley, 2nd Edition, 2007
 2. 'Antennas and Wave Propagation', J.D. Krauss, McGraw Hill TMH, 4th Edition, 2010
- 'Antennas and propagation', A.R. Harish, M. Sachidanada, Pearson Education, 2015

Web links and Video Lectures (e-Resources):

<https://www.youtube.com/watch?v=flbdW0NGIU0>

<https://nptel.ac.in/courses/117107035>

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Different types of antenna synthesis or technical seminar on advanced types of antennas.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
C01	Classify different types of antennas	Understand
C02	Define and illustrate various types of array antennas	Understand
C03	Design antennas like Yagi-Uda, Helical antennas and other broadband antennas	Analyse
C04	Describe different antenna synthesis methods	Understand
C05	Apply methods like Method of Moments, Pocklington's integral equation, Source modeling.	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research/investigation and development work to solve practical problems	PO1
2	An ability to write and present a substantial technical report/document	PO2
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	PO3
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	PO4
5	An ability to apply Professional ethics, responsibilities and norms of the engineering	PO5
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain	PO6

Mapping of COS and POs

	PO1	PO2	PO3	PO4	PO5	PO6
C01	-	-	-	-		-
C02	-	-	-	-		-
C03	-	-	-	-		-
C04	-	-	-	-		-
C05	-	-	-	-		-

DIGITAL VLSI DESIGN			
Course Code	MLEL202	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours Theory	Total Marks	100
Credits	03	Exam Hours	03
Course Learning Objectives: - To understand the operation of MOS transistor, Scaling and Small Geometry Effects. - To study Static Characteristics, Switching Characteristics and Interconnect Effect of MOS Inverter. - To provide the insight of Semiconductor Memories, Dynamic Logic Circuits and BiCMOS Logic Circuits. - To know Chip Input and Output Circuits, Clock Generation and Distribution Circuits, Design for Manufacturability.			
Module-1			
MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.			
RBT Levels: L2, L3			
Module-2			
MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n-Type MOSFET Load, CMOS Inverter.			
RBT Levels: L2, L3			
Module-3			
Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits.			
RBT Levels: L2, L3			
Module-4			
Semiconductor Memories: Introduction, Dynamic Random-Access Memory (DRAM), Static Random-Access Memory (SRAM).			
RBT Levels: L2, L3			
Module-5			
BiCMOS Logic Circuits: Introduction, BiCMOS Applications. Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.			
RBT Levels: L2, L3			
Practical Component of PCC: Conduct the experiments using Cadence/ Mentor Graphics / Xilinx ISE System Edition 14.7/ XUP SPARTAN 3E Kit with USB Programming cable			
Sl. No.	Experiments		
1	To plot the (i) output characteristics & (ii) transfer characteristics of an n-channel and p-channel MOSFET.		
2	To design and plot the static (VTC) and dynamic characteristics of a digital CMOS inverter.		
3	To design and plot the dynamic characteristics of 2-input NAND, NOR, XOR and XNOR logic gates using CMOS technology.		
4	To design and plot the characteristics of a 4x1 digital multiplexer using pass transistor logic.		
5	To design and plot the characteristics of a positive and negative latch based on multiplexers.		
6	To design and plot the characteristics of a master-slave positive and negative edge triggered registers based on multiplexers		
7	To Design D, T, JK Flip Flops		
8	To Design BCD adder		

9	To Design ALU															
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.																
Continuous Internal Evaluation: 1. Three Unit Tests each of 20 Marks 2. Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks CIE methods /question paper is designed to attain the different levels of Bloom’s taxonomy as per the outcome defined for the course.																
Semester End Examination: 1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50. 2. The question paper will have ten full questions carrying equal marks. 3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module. 4. Each full question will have a sub-question covering all the topics under a module. 5. The students will have to answer five full questions, selecting one full question from each module 																
Suggested Learning Resources: Books 1. “Sung Mo Kang & Yusuf Leblebici”, CMOS Digital Integrated Circuits: Analysis and Design, Tata McGraw-Hill, Third Edition. 2. “Neil Weste and K. Eshraghian”, Principles of CMOS VLSI Design: A System Perspective Pearson Education (Asia) Pvt. Ltd. Second Edition, 2000. 3. “Wayne, Wolf”, Modern VLSI Design: System on Silicon, Prentice Hall PTR/ Pearson Education Second Edition, 1998 4. “Douglas A Pucknell& Kamran Eshraghian”, Basic VLSI Design PHI 3rd Edition																
Web links and Video Lectures (e-Resources): 1. https://www.youtube.com/watch?v=57uTCtSQV50&list=PLHO2NKv71TvsSqYwVvUCZwNkY-jUyUHdS 2. https://www.youtube.com/watch?v=oL8SKNxEdHs&list=PLLy_2iUCG87Bdulp9brz9AcvW_TnFCUmM																
Course outcome (Course Skill Set) At the end of the course the student will be able to: <table><tr><th>Sl. No.</th><th>Description</th><th>Blooms Level</th></tr><tr><td>CO1</td><td>Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.</td><td>L4</td></tr><tr><td>CO2</td><td>Analyse the Switching Characteristics in Digital Integrated Circuits.</td><td>L4</td></tr><tr><td>CO3</td><td>Use the Dynamic Logic circuits in state-of-the-art VLSI chips.</td><td>L3</td></tr><tr><td>CO4</td><td>Interpret critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon</td><td>L2</td></tr></table>		Sl. No.	Description	Blooms Level	CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.	L4	CO2	Analyse the Switching Characteristics in Digital Integrated Circuits.	L4	CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	L3	CO4	Interpret critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	L2
Sl. No.	Description	Blooms Level														
CO1	Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.	L4														
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CO3	Use the Dynamic Logic circuits in state-of-the-art VLSI chips.	L3														
CO4	Interpret critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon	L2														
Suggested Learning Resources: Text Books 1. Digital Signal Processing Principles, Algorithms, and Applications by John G. Proakis, Prentice-Hall International Inc., 4th Edition, 2012. 2. Theory and Application of Digital Signal Processing by Lawrence R. Rabiner and Bernard Gold. Reference Books																

1. Oppenheim, Alan V. Discrete-time signal processing. Pearson Education India, 1999.
2. Mitra, Sanjit Kumar, and Yonghong Kuo. Digital signal processing: a computer-based approach. Volume 2. New York: McGraw-Hill Higher Education, 2006.

Web links and Video Lectures (e-Resources):

1. <https://ekeeda.com/degree-courses/electrical-engineering/advanced-digital-signal-processing>
2. <https://dss-kiel.de/index.php/teaching/lectures/lecture-advanced-digital-signal-processing>

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Able to analyze and implement the frequency analysis & correlation of discrete-time linear time invariant systems.	L4
CO2	Able to implement sampling rate conversion by decimation & Interpolation process and design digital filter banks	L4
CO3	Able to analyze forward and backward linear prediction of a stationary random process using Levinson-Durbin Algorithm	L4
CO4	Able to understand and analyze adaptive filters and its application using LMS algorithm & RLS algorithm.	L4
CO5	Able to understand and analyze adaptive filters and its application using LMS algorithm & RLS algorithm.	L4

ADVANCED COMMUNICATION SYSTEMS			
Course Code	MLEL203	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40 Hours of teaching	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: This course will enable students: - To understand the concept of low pass and Band pass signals during modulation at the Transmitter. - To analyze the Receiver performance for various types of single carrier symbol modulations through ideal and AWGN channels. - To apply single carrier equalizers for various modulation schemes and detection methods for defined channel models - To understand the concepts of synchronization for carrier and symbol timing recovery at receiver. - To understand the concepts of spread spectrum systems for communications in a Jamming, multiuser and low power intercept environment.			
Module-1			
Signal Representation: Low pass representation of band pass signals, Low pass representation of band pass random process. Modulation: Representation of digitally modulated Signals, Modulation Schemes without memory (Band Limited Schemes - PAM, BPSK, QPSK, MPSK, MQAM, Power Limited Schemes – FSK, MFSK, DPSK, DQPSK), modulation schemes with memory (Basics of CPFSK and CPM – Full Treatment of MSK), Transmit PSD for Modulation Schemes.			
RBT Levels: L2, L3			
Module-2			
Demodulation: Vector Channel, Vector Channel +AWGN, Performance parameters, Optimum Coherent Detection for power limited and Band limited schemes, Optimal Coherent detection for schemes with memory, Optimal Non- Coherent detection for schemes without and with memory (FSK, DPSK, DQPSK), Comparison of detection schemes.			
RBT Levels: L2, L3			
Module-3			
Bandlimited Channels: Band limited channel characterization, signalling through band limited linear filter channels, Sinc, RC, Duobinary and Modified Duobinary signalling schemes. Linear Equalizers: Zero forcing Equalizer, MSE and MMSE. Non-Linear Equalizers: Decision - feedback equalization, Predictive DFE, Performance of DFE. Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer.			
RBT Levels: L2, L3			
Module-4			
Synchronization – Signal Parameter estimation, Carrier Phase Estimation, Symbol Timing Recovery, Performance of ML estimators. Fading – Large scale, small scale; Statistical characterization of multipath channels – Delay and Doppler spread, classification of multipath channels, Binary signalling over frequency non selective Rayleigh fading channel.			
RBT Levels: L2, L3			
Module-5			
Spread Spectrum Signals For Digital Communication: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals, generation of PN sequences, Frequency hopped spread spectrum signals, Time hopping SS, Synchronization of SS systems.			
RBT Levels: L2, L3			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Books**

1. 'Digital Communications', John G. Proakis, Masoud Salehi, Pearson Education, ISBN:978-9332535893, 5th edition, 2014
2. Digital Communications: Fundamentals and Applications: Fundamentals & Applications', Bernard Sklar, Pearson Education, ISBN:9788131720929, 2nd edition, 2009
3. 'Digital Communications Systems', Simon Haykin, Wiley, ISBN:9788126542314, 1st edition, 2014

Massive Open Online Courses:

1. Modern Digital Communication Techniques-By Prof. Suvra Sekhar Das | IIT Kharagpur
2. Principles of Signal Estimation for MIMO/ OFDM Wireless Communication-By Prof. Aditya K. Jagannatham | IIT Kanpur

Skill Development Activities Suggested

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities,

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
C01	Explain the concept of low pass and Bandpass signals representations at the Transmitter, process of Detection and Estimation at the receiver in the presence of AWGN only.	L2
C02	Evaluate Receiver performance for various types of single carrier symbol modulations through ideal and AWGN Non-bandlimited and bandlimited channels.	L3
C03	Design single carrier equalizers for various symbol modulation schemes and detection methods for defined channel models, and compute parameters to meet desired rate and performance requirements.	L4
C04	Explain the concepts of multi-channel signaling scheme and synchronization for carrier and symbol timing recovery at receiver.	L2
C05	Design and Evaluate Non band limited and Non power limited spread spectrum systems for communications in a Jamming environment, multiuser situation and low	L4

REAL TIME OPERATING SYSTEM			
Course Code	MLEL204	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours of teaching	Total Marks	100
Credits	3	Exam Hours	03
Course Learning objectives: - To understand a typical embedded system and its constituents - To learn the selection process of processor and memory for the embedded systems - To learn communication buses and protocols used in the embedded and real-time systems - To understand real-time operating system and the types of RTOS - To learn various approaches to real-time scheduling - To learn software development process and tools for RTOS applications			
Module-1			
Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Re-entrant Functions.			
RBT Levels: L2, L3			
Module-2			
Processing with Real Time Scheduling: Scheduler Concepts, Pre-emptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy.			
RBT Levels: L2, L3			
Module-3			
Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software.			
RBT Levels: L2, L3			
Module-4			
Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, checking return codes, Single-step debugging, Test access ports, Trace Ports.			
RBT Levels: L2, L3			
Module-5			
Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving intertask /thread communication.			
RBT Levels: L2, L3			
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.			
Continuous Internal Evaluation: - Three Unit Tests each of 20 Marks - Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.			
Semester End Examination: The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to			

50.

- 2) The question paper will have ten full questions carrying equal marks.
- 3) Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
- 4) Each full question will have a sub-question covering all the topics under a module.
- 5) The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Textbooks:

1. 'Real-Time Embedded Systems and Components', Sam Siewert, Cengage Learning, India Edition, 2007.
2. 'Embedded/Real Time Systems, Concepts, Design and Programming, Black Book', Dr. K.V.K.K Prasad, Dream Tech Press, New edition, 2010.

Reference Books:

1. 'Real Time System', James W S Liu, Pearson Education, 2008.
2. 'Programming for Embedded Systems', Dream Tech Software Team, John Wiley, India Pvt. Ltd., 2008.

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Recognize and classify real-time systems	L2
CO2	Apply software development process to a given RTOS application	L2
CO3	Design a given RTOS based application	L3
CO4	Ability to use commercial tools to develop RTOS based applications	L3

CMOS RF CIRCUIT DESIGN			
Course Code	MLEL215A	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours of teaching	Total Marks	100
Credits	03	Exam Hours	3
Course Learning Objectives: - To provide understanding of designing RF integrated circuits in state-of-the-art CMOS technology. - To study transceiver, Low Noise Amplifiers, PLLs and other related concepts and circuits.			
Module-1			
Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion.			
RBT Levels: L2, L3			
Module-2			
Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.			
RBT Levels: L2, L3			
Module-3			
Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.			
RBT Levels: L2, L3			
Module-4			
Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.			
RBT Levels: L2, L3			
Module-5			
VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design.			
RBT Levels: L2, L3			
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.			
Continuous Internal Evaluation: - Three Unit Tests each of 20 Marks - Two assignments each of 20 Marks or one Skill Development Activity of 40 marks to attain the COs and POs The sum of three tests, two assignments/skill Development Activities, will be scaled down to 50 marks CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.			
Semester End Examination:			

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

1. B. Razavi, "RF Microelectronics" second edition, PHI
2. R. Jacob Baker, H.W. Li, D.E. Boyce, "CMOS Circuit Design, layout and Simulation" PHI 1998
3. Thomas H. Lee, "Design of CMOS RF Integrated Circuits" Cambridge University press 1998
4. Y.P. Tsividis, "Mixed Analog and Digital Devices and Technology", TMH 1996

Web links and Video Lectures (e-Resources):

1. <https://nptel.ac.in/courses/108106105>
2. <https://www.youtube.com/watch?v=T0Kbt7CcqUA&list=PLQorUaRee4AEeyuqnpysZcGT4FFgRdkuM>

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Analyze the effect of nonlinearity and noise in RF and microwave design.	L4
CO2	Exemplify the approaches taken in actual RF products	L2
CO3	Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.	L3
CO4	Explain various receivers and transmitter topologies with their merits and drawbacks.	L2
CO5	Demonstrate how the system requirements define the parameters of the circuits and	L2

STATISTICAL SIGNAL PROCESSING			
Course Code	MLEL215B	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40HoursTheory	Total Marks	100
Credits	3	Exam Hours	03
Course Objectives: This course will enable students: - Understand random processes and its properties - Understand the basic theory of signal detection and estimation - Identify the engineering problems that can be put into the frame of statistical signal processing - Solve the identified problems using the standard techniques learned through this course. - Make contributions to the theory and the practice of statistical signal processing.			
Module-1			
Random Processes: Random variables, random processes, white noise, filtering random processes, spectral factorization, ARMA, AR and MA processes (Text1). RBT Levels: L2, L3			
Module-2			
Signal Modeling: Least squares method, Padé approximation, Prony's method, finite data records, stochastic models, Levinson-Durbin recursion, Schur recursion, Levinson recursion (Text1). RBT Levels: L2, L3			
Module-3			
Spectrum Estimation: Nonparametric methods, minimum-variance spectrum estimation, maximum entropy method, parametric methods, frequency estimation, principal component spectrum estimation (Text1). RBT Levels: L2, L3			
Module-4			
Optimal and Adaptive Filtering: FIR and IIR Wiener filters, Discrete Kalman filter, FIR Adaptive filters: Steepest descent, LMS, LMS-based algorithms, adaptive recursive filters, RLS algorithms (Text1). RBT Levels: L2, L3			
Module-5			
Array Processing: Array fundamentals, beam-forming, optimum array processing, performance considerations, adaptive beam-forming, linearly constrained minimum-variance beam-formers, side-lobe cancellers. (Text2). RBT Levels: L2, L3			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Textbooks:**

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & Sons (Asia) Pvt. Ltd., 2002.
2. Dimitris G. Manolakis, Vinay K. Ingle, and Stephen M. Kogon, "Statistical and Adaptive Signal Processing : Spectral Estimation, Signal Modeling, Adaptive Filtering and Array Processing", McGraw-Hill International Edition, 2000.

Web links and Video Lectures (e-Resources):

nptel.ac.in

Skill Development Activities Suggested

- Mathematical modeling of signals: linear vs. nonlinear, deterministic signals, random signals, unknown parameters.
- Mathematical modeling of noise: white Gaussian noise, coloured Gaussian noise, general Gaussian noise, IID non-Gaussian noise.
- Specific algorithms for estimation, detection, and spectral estimation: parameter estimation, signal extraction, adaptive filtering, sinusoidal estimation, matched filters, estimator-correlator, spectral estimation via Fourier and high-resolution methods.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
C01	Design statistical DSP algorithm to meet desired needs	Analyze
C02	Apply vector space methods to statistical signal processing problems	Apply
C03	Identify the engineering problems that can be put into the frame of statistical signal processing	Understand
C04	Understand Wiener filter theory and design discrete and continuous Wiener filters	Understand
C05	Understand Kalman Filter theory and design discrete Kalman filters	Understand

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research/investigation and development work to solve practical problems	P01
2	An ability to write and present a substantial technical report/document	P02
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	P03
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	P04
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	P05
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain.	P06

Mapping of COS and POs

	P01	P02	P03	P04	P05	P06
C01	-	-	-	-		-
C02	-	-	-		-	-
C03	-	-		-	-	-
C04	-	-	-			-
C05	-	-	-	-		-

PROBABILITY AND RANDOM PROCESS			
Course Code	MLEL215C	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40HoursTheory	Total Marks	100
Credits	3	Exam Hours	03
Course Objectives: This course will enable students: - To understand Discrete and Continuous Random variables, Random Processes and their applications in Electronic Transmissions. - To apply concepts of Probability to solve problems in communication Engineering. - To find functional relationship between random inputs and outputs with the use of Random Process Techniques - Analyze about the correlation Functions.			
Module-1			
Probability and Random Variable Probability: Set theory, Experiments and Sample Spaces, Discrete and Continuous Sample Spaces, Events, Probability Definitions and Axioms, Mathematical Model of Experiments, Joint Probability, Conditional Probability, Total Probability, Bayes' Theorem, and Independent Events, Bernoulli's trials. The Random Variable: Definition of a Random Variable, Conditions for a Function to be a Random Variable, Discrete and Continuous, Mixed Random Variable. RBT Levels: L2, L3			
Module-2			
Distribution and density functions and Operations on One Random Variable Distribution and density functions: Distribution and Density functions, Properties, Binomial, Poisson, Uniform, Exponential Gaussian, Rayleigh and Conditional Distribution, Methods of defining Conditioning Event, Conditional Density function and its properties, problems. Operation on One Random Variable: Expected value of a random variable, function of a random variable, moments about the origin, central moments, variance and skew, characteristic function, moment generating function, transformations of a random variable, monotonic transformations for a continuous random variable, non-monotonic transformations of continuous random variable, transformations of Discrete random variable. RBT Levels: L2, L3			
Module-3			
Multiple Random Variables and Operations on Multiple Random Variables Multiple Random Variables: Vector Random Variables, Joint Distribution Function and Properties, Joint density Function and Properties, Marginal Distribution and density Functions, conditional Distribution and density Functions, Statistical Independence, Distribution and density functions of Sum of Two Random Variables and Sum of Several Random Variables, Central Limit Theorem- Unequal Distribution, Equal Distributions Operations on Multiple Random Variables: Expected Value of a Function of Random Variables, Joint Moments about the Origin, Joint Central Moments, Joint Characteristic Functions, and Jointly Gaussian Random Variables: Two Random Variables case and N Random Variable case, Properties, Transformations of Multiple Random Variables. RBT Levels: L2, L3			
Module-4			
Stochastic Processes-Temporal Characteristics: The Stochastic process Concept, Classification of Processes, Deterministic and Nondeterministic Processes, Distribution and Density Functions, Statistical Independence and concept of Stationarity: First-Order Stationary Processes, Second Order and Wide-Sense Stationarity, Nth-Order and Strict-Sense Stationarity, Time Averages and Ergodicity, Mean-Ergodic Processes, Correlation-Ergodic Processes Autocorrelation Function and Its Properties, Cross-Correlation Function and Its Properties, Covariance Functions and its properties, Gaussian Random Processes. Linear system Response: Mean and Mean-squared value, Autocorrelation, Cross-Correlation Functions.			

RBT Levels: L2, L3
Module-5
Stochastic Processes-Spectral Characteristics: The Power Spectrum and its Properties, Relationship between Power Spectrum and Autocorrelation Function, the Cross-Power Density Spectrum and Properties, Relationship between Cross-Power Spectrum and Cross-Correlation Function. Spectral characteristics of system response: power density spectrum of response, cross power spectral density of input and output of a linear system. RBT Levels: L2, L3
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. Continuous Internal Evaluation: 1. Two Unit Tests each of 25 Marks 2. Two assignments each of 25 Marks or one Skill Development Activity of 50 marks to attain the COs and POs The sum of two tests, two assignments/skill Development Activities, will be scaled down to 50 marks CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course. Semester-End Examination: 1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50. 2. The question paper will have ten full questions carrying equal marks. 3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module. 4. Each full question will have a sub-question covering all the topics under a module. 5. The students will have to answer five full questions, selecting one full question from each module
Suggested Learning Resources: Textbooks: 1. Probability, Random Variables & Random Signal Principles -Peyton Z. Peebles, TMH, 4th Edition, 2001. 2. Probability and Random Processes-Scott Miller, Donald Childers, 2nd Edn, Elsevier, 2012
Web links and Video Lectures (e-Resources):
Nptel.ac.in
Skill Development Activities Suggested ● Online certification courses on probability and random process. ● Mini projects can be suggested on the related area.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
C01	understand Discrete and Continuous Random variables, Random Processes and their applications in Electronic Transmissions	Understand
C02	To apply concepts of Probability to solve problems in Communication Engineering.	Apply
C03	To find functional relationship between random inputs and outputs with the use of Random Process Techniques	Apply
C04	Analyse about the correlation Functions	Analyse

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research/investigation and development work to solve practical problems	P01
2	An ability to write and present a substantial technical report/document	P02
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	P03
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	P04
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	P05
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain.	P06

Mapping of COS and POs

	P01	P02	P03	P04	P05	P06
C01	-		-	-		-
C02	-		-	-		-
C03	-		-	-		-
C04	-		-	-		-

SIMULATION,MODELLING AND ANALYSIS			
Course Code	MLEL215D	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	(3:0:0)	SEE Marks	50
Total Hours of Pedagogy	40HoursTheory	Total Marks	100
Credits	3	Exam Hours	03
Course Objectives: Thiscoursewillenablestudents: • Definethebasicsofsimulationmodellingandreplicatingthepacticalsituationsinorganizations • Generaterandomnumbersandrandomvariatesusingdifferenttechniques. • Developsimulationmodelusingheuristicmethods. • AnalysisofSimulationmodelsusinginputanalyzer,andoutputanalyzer. • ExplainVerificationandValidationofsimulationmodel.			
Module-1			
BasicSimulationModeling: Natureofsimulation,Systems,ModelsandSimulation,Discrete-EventSimulation,SimulationofSingleServer Queuing System, Simulation of inventory system, Parallel and distributed simulation and the high levelarchitecture, Steps in sound simulation study, and Other types of simulation, Advantages and disadvantages.(1.1, 1.2,1.3,1.4,1.4.1, 1.4.2, 1.4.3, 1.5,1.5.1,1.5.2, 1.6, 1.7,1.8, 1.9) RBT Levels: L2, L3			
Module-2			
Review of Basic Probability and Statistics: Random Variables and their properties, Simulation Output DataandStochasticProcesses,EstimationofMeans,VariancesandCorrelations,ConfidenceIntervalsandHypothesistests for the Mean. Buildingvalid,credibleandappropriatelydetailedsimulationmodels: Introductionanddefinitions,Guidelinesfordeterminingthelevelofmodelsdetail,Management'sRoleintheSimulationProcess,Techniques for increasing model validity and credibility, Statistical procedure for comparing the real worldobservationsandsimulationoutputdata.(4.2, 4.3, 4.4,4.5, 5.1, 5.2, 5.4,5.5, 5.6,5.6.1, 5.6.2) RBT Levels: L2, L3			
Module-3			
Selecting Input Probability Distributions: Useful probability distributions, activity I, II and III. Shifted andtruncated distributions; Specifying multivariate distribution, correlations, and stochastic processes; Selectingthedistributionintheabsenceofdata,Models of arrival process. (6.2, 6.4,6.5, 6.6,6.8,6.10,6.11, 6.12) RBT Levels: L2, L3			
Module-4			
RandomNumberGenerators: LinearcongruentialGenerators,Otherkinds,Testingnumbengenerators, GeneratingtheRandomVariates: Generalapproaches,generatingcontinuousrandomvariates,generatingdiscreterandomvariates,generatingrandomvectors,andcorrelatedrandomvariates;Generatingarrivalprocesses.(7.2,7.3,7.4,8.2,8.3,8.4,8.5, 8.6) RBT Levels: L2, L3			
Module-5			
Outputdataanalysisforasinglesystem: Transient and steady state behavior of a stochastic process; Types of simulations with regard to analysis;Statisticalanalysisforterminating simulation;Statisticalanalysisforsteadystateparameters;Statisticalanalysisforsteadystatecycleparameters;Multiplemeasuresofperformance,Timeplotsofimportant variables. RBT Levels: L2, L3			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of two tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:**Textbooks:**

1. Averill Law, "Simulation modeling and analysis", McGraw Hill 4th edition, 2007.

Reference Books:

1. Tayfur Altioek and Benjamin Melamed, "Simulation modeling and analysis with ARENA", Elsevier, Academic press, 2007.
2. Jerry Banks, "Discrete event system Simulation", Pearson, 2009
3. Seila Ceric and Tadikamalla, "Applied simulation modeling", Cengage, 2009.
4. George S. Fishman, "Discrete event simulation", Springer, 2001.
5. Frank L. Severance, "System modeling and simulation", Wiley, 2009..

Web links and Video Lectures (e-Resources):

Nptel.ac.in

Skill Development Activities Suggested

- Online certification courses.
- Mini projects can be suggested on the related area.

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

Sl. No.	Description	Blooms Level
C01	Describe the role of important elements of discrete event simulation and modeling paradigm	Understand
C02	Conceptualize real world situations related to systems development decisions, originating from source requirements and goals.	Analyze
C03	Develop skills to apply simulation software to construct and execute goal-driven system models.	Analyze
C04	Interpret the model and apply the results to resolve critical issues in a real world environment.	Apply

Program Outcome of this course

Sl. No.	Description	POs
1	An ability to independently carry out research/investigation and development work to solve practical problems	P01
2	An ability to write and present a substantial technical report/document	P02
3	Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program	P03
4	An ability to create, select, apply appropriate techniques, resources and modern tools to solve complex engineering activities with an understanding of their limitations.	P04
5	An ability to apply Professional ethics, responsibilities and norms of the engineering.	P05
6	An ability to recognize the need to engage in independent and life-long learning in Digital Communication and Networking domain.	P06

Mapping of COS and POs

	P01	P02	P03	P04	P05	P06
C01	-	-	-	-		
C02	-	-	-	-		-
C03	-	-	-			-
C04	-	-	-	-		-

MECHATRONICS			
Course Code	MLEL216A	CIE Marks	50
Teaching Hours/Week (L:P: SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours of teaching	Total Marks	100
Credits	03	Exam Hours	03
Course Learning objectives: - To understand the basics of Mechatronics and its design approach. - To understand the operation and applications of various sensors. - To understand the operation of various actuators and their applications in systems. - To understand the concepts of logic design, computer communication networks and Fault diagnosis and Analysis in Mechatronic Systems. - To understand the concepts of data acquisition, software design and development.			
Module-1			
Overview of mechatronics: What is Mechatronics? Integrated Mechatronic Design Approach, System Interfacing, Embedded Systems, Instrumentation and Control Systems, Open and closed loop systems, importance of feedback systems, Transfer function, Microprocessor Based Controllers and Microelectronics. An Introduction to Micro-technology and Nanotechnology, Mechatronics: Miniaturized, Examples and applications.			
RBT Levels: L2, L3			
Module-2			
Sensors and application: Introduction to Sensors, Classification of sensors, Sensor – Static and Dynamic Characteristics, Sensors, Linear and Rotational Sensors, Acceleration Sensors, Force Measurement, Torque and Power Measurement, Flow Measurement, Temperature Measurements, Distance Measuring and Proximity Sensors, Light Detection, Use of RF, Infra-Red sensors in automobiles, Micro-sensors.			
RBT Levels: L2, L3			
Module-3			
Actuators: Introduction to Actuators – Mechanical, Electrical and combinational actuators, Electro-mechanical Actuators, Electrical Machines, Piezoelectric Actuators, Hydraulic and Pneumatic Actuation Systems, Applications of few types of actuators in automobiles. Electrical Actuation Systems: Importance of actuators, classification of Actuators, Mechanical Switches, Bouncing and De-bouncing in Mechanical Switches, Solid State Switches: transistors, Darlington pair, Thyristors, Triacs.			
RBT Levels: L2, L3			
Module-4			
Computers and Logic Systems: Logic System Design, Synchronous and Asynchronous Systems, Sequential Systems, Control System Architecture, Control with Embedded Computers and Programmable Logic Control, Digital Signal Processing for Mechatronic Applications, Neural Networks and Fuzzy Systems, Artificial Intelligence and Expert System Approach to control System design, Design Optimization of Mechatronic Systems.			
RBT Levels: L2, L3			
Module-5			
Data Acquisition and Software Development: Introduction to Data Acquisition, Measurement, Techniques, Data Acquisition systems, Importance of data acquisition in automobiles. Computer-Based Instrumentation Systems, Software Design and Development, Data Recording and Data Logging, DAQ for automotive engine system and other Measurements, Electronic Control Unit (ECU), Features of design and system logic in multiple signal measurements.			
RBT Levels: L2, L3			
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum			

total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module

Suggested Learning Resources:

Text Books

1. Mechatronics – W.Bolton, Longman, 2Ed, Pearson Publications, 2007
2. Microprocessor Architecture, Programming & Applications With 8085/8085A – R.S. Ganokar, Wiley Eastern, 2008

Reference Books

1. Mechatronics – Principles, Concepts and Applications – Nitiagour and PremchandMohalik – Tata McGraw Hill – 2003.
2. Measurement, Instrumentation, and Sensors Handbook - John G. Webster. Editor-in-chief, CRC Press. 1999. 0-8493-2145-X. PDF files online available at www.engnetbase.com
3. Mechatronics Principles & Applications by Godfrey C. Onwubolu, Elsevier.
4. Introduction Mechatronics & Measurement Systems, David.G. Aliciatore

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Students and the course instructor/s to involve either individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Explain the basics of Mechatronics and its design approach.	L3
CO2	Explain the operation and applications of various sensors.	L3
CO3	Explain and discuss the operation of various actuators and their applications in	L4

	systems.	
C04	Explain and discuss the concepts of logic design, computer communication networks and Fault diagnosis and Analysis in Mechatronic Systems.	L4
C05	Explain and discuss the concepts of data acquisition, software design and development.	L4

INTERNET OF THINGS AND APPLICATIONS			
Course Code	MLEL216B	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40HoursTheory	Total Marks	100
Credits	3	Exam Hours	03
Course Learning objectives: This Course will enable students to - Understand IoT concepts and network architecture for practical application. - Understand roles in IoT, simplified architecture, and computing hierarchy. - Understand smart objects, sensor networks, and IoT access technologies. - Gain knowledge about IoT application protocols, data analytics, and big data technologies. - Understand IoT security strategies and best practices.			
Module-1			
What is IoT: Introduction to IoT, Genesis of IoT, IoT and Digitization , IoT Impact, Convergence of IT and OT ,IoT Challenges IoT Network Architecture and Design: Drivers Behind New Network Architectures, Comparing IoT Architectures RBT Levels: L2, L3			
Module-2			
Simplified IoT Architecture: The Core IoT Functional Stack, Layer1, Layer 2, Layer3. IoT Data Management and Compute Stack: Fog Computing, Edge Computing, The Hierarchy of Edge, Fog and Cloud. RBT Levels: L2, L3			
Module-3			
Smart Objects: The “Things” in IoT: Sensors, Actuators and Smart Objects, Micro-Electro-Mechanical Systems (MEMS),Smart Objects, Sensor Networks. Connecting Smart Objects: Communications Criteria, Range, Frequency Bands, Power Consumption, Topology, Constrained Devices, Constrained-Node Networks, Data Rate and Throughput, Latency and Determinism, Overhead and Payload. IoT Access Technologies: IEEE 802.15.4, Standardization and Alliances, Physical Layer, MAC Layer, Topology, Security, Competitive Technologies, IEEE 802.15.4g and 802.15.4e, Standardization and Alliances, Physical Layer, MAC Layer, Topology, Security, Competitive Technologies. RBT Levels: L2, L3			
Module-4			
Application Protocols for IoT: The Transport Layer, IoT Application Transport Methods, Application Layer Protocol Not Present, SCADA, A Little Background on SCADA, Adapting SCADA for IP, Tunneling Legacy SCADA over IP Networks, SCADA Protocol Translation, SCADA Transport over LLNs with MAP-T, Generic Web-Based Protocols. Data and Analytics for IoT: An introduction to Data Analytics for IoT, Big Data Analytics Tools and Technology, Edge Streaming Analytics RBT Levels: L2, L3			
Module-5			
Securing IoT: A Brief History of OT Security, Common Challenges in OT Security, How IT and OT Security Practices and Systems Vary, Formal Risk Analysis Structures, The Phased Application of Security in an Operational Environment. RBT Levels: L2, L3			

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Two Unit Tests each of **25 Marks**
2. Two assignments each of **25 Marks** or **one Skill Development Activity of 50 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module.

Suggested Learning Resources:**Text Books:**

1. David Hanes , Gonzalo Salgueiro, Patrick Grossetete , Robert Barton , Jerome Henry "IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things".

Reference books:

1. Arshdeep Bhaga, Vijay Madishetti, "Internet of things: A hands on Approach", Universities Press, ISBN:978172719547, 2015.

Web links and Video Lectures (e-Resources):

- <https://youtu.be/c6lqXb14c0I>

Skill Development Activities Suggested

- The students with the help of the course teacher can take up relevant technical – activities which will enhance their skill.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description
CO1	Explain IoT concepts and network architecture for practical application.
CO2	Analyse roles in IoT, apply simplified architecture and computing hierarchy.
CO3	Analyse smart objects, sensor networks, and IoT access technologies.
CO4	Analyze and apply IoT application protocols, data analytics, and big data technologies.
CO5	Explain IoT security strategies and apply best practices effectively.

Program Outcome of this course

Sl. No.	Description	POs
1	Adequate knowledge of fundamentals on sensors, signal conditioning and IoT.	P01
2	Ability to design, implement, analyse, interpret data and synthesis of information.	P02
3	Ability to analyse a problem critically using scientific approach, relevant IT tools and techniques.	P03
4	Appropriate research skills for solving new problem and present a substantial technical report.	P04
5	Ability to work ethically and carry out the work with social responsibility.	P05
6	Professional skills to carry out work independently or collaboratively in a multidisciplinary environment.	P06

Mapping of COS and POs

	P01	P02	P03	P04	P05	P06
C01	X	X				
C02	X	X				
C03	X	X	X			X
C04	X	X	X			X
C05	X				X	

CYBER SECURITY			
Course Code	MLEL216C	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours of teaching	Total Marks	100
Credits	3	Exam Hours	03
Course Learning objectives: - To understand the cybercrime and laws and computer forensics - To explain the phishing and identity theft			
Module-1			
Introduction to Cybercrime and Laws Introduction, Cybercrime: Definition and Origins of the word, Cybercrime and information Security, Who are Cybercriminals? Classification of Cybercrimes. How Criminals Plan Them – Introduction, How Criminals Plan the Attacks, Cybercafé and Cybercrimes, Botnets, Attack Vector, The Indian IT Act 2008 and amendments.			
RBT Levels: L2, L3			
Module-2			
Tools and Methods used in Cybercrime Introduction, Proxy Server and Anonymizers, Password Cracking, Keyloggers and Spyware, Virus and Worms, Trojan and backdoors, Steganography, DOS and DDOS attack, SQL injection, Buffer Overflow.			
RBT Levels: L2, L3			
Module-3			
Phishing and Identity Theft Introduction, Phishing – Methods of Phishing, Phishing Techniques, Phishing Toolkits and Spy Phishing. Identity Theft – PII, Types of Identity Theft, Techniques of ID Theft. Digital Forensics Science, Need for Computer Cyber forensics and Digital Evidence, Digital Forensics Life Cycle.			
RBT Levels: L2, L3			
Module-4			
Understanding Computer Forensics: Introduction, Historical Background of Cyber forensics, Digital Forensics Science, The Need for Computer Forensics, Cyber forensics and Digital Evidence, Forensics Analysis of E-Mail, Digital Forensics Life Cycle, Chain of Custody Concept, Network Forensics, Approaching a Computer Forensics Investigation, Setting up a Computer Forensics Laboratory : Understanding the Requirements, Computer Forensics and Steganography, Relevance of the OSI 7 Layer Model to Computer Forensics, Forensics and Social Networking Sites: The Security/Privacy Threats, Computer Forensics from Compliance Perspective, Challenges in Computer Forensics, Special Tools and Techniques, Forensics Auditing, Antiforensics.			
RBT Levels: L2, L3			
Module-5			
Introduction to Security Policies and Cyber Laws: Need for An Information Security Policy, Information Security Standards Iso, Introducing Various Security Policies and Their Review Process, Introduction to Indian Cyber Law, Objective and Scope of the IT Act, 2000, Intellectual Property Issues, Overview of Intellectual -Property - Related Legislation in India, Patent, Copyright, Law Related to Semiconductor Layout and Design, Software License.			
RBT Levels: L2, L3			
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.			
Continuous Internal Evaluation:			

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks** to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.
3. Each full question is for 20 marks. There will be two full questions (with a maximum of four sub-questions) from each module.
4. Each full question will have a sub-question covering all the topics under a module.
5. The students will have to answer five full questions, selecting one full question from each module

Suggested Learning Resources:

Text Books

1. Anti-HackerToolKit(IndianEdition)byMikeShema,PublicationMcGrawHill.
2. CyberSecurityUnderstandingCyberCrimes,ComputerForensicsandLegalPerspectivesbyNinaGodbolean dSunitBelpure,PublicationWiley.
3. Introductiontoinformationsecurityand cyberlaws SuryaPrakashTripathi,RitendraGoyal,Praveen Kumar Shukla DreamtechPress 2015
4. MarjieT. Britz- Computer Forensics and Cyber Crime: An Introduction - Pearson
5. Chwan-Hwa(John)Wu,J.DavidIrwin-IntroductiontoComputerNetworksandCybersecurity CRC Press
6. BillNelson,AmeliaPhillips,ChristopherSteuart-GuidetoComputerForensicsandInvestigations CengageLearning

Web links and Video Lectures (e-Resources):

1. <https://www.mooc.org/>
2. <https://onlinecourses.nptel.ac.in/>

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
CO1	Able to understand the cyber crime and cyber laws	L2
CO2	Able to understand and analyze the tools and methods used in cyber crime	L2 L4
CO3	Able to understand and analyze the phishing and identity, computer forensics	L2 L4

AUTOMOTIVE ELECTRONICS			
Course Code	MLEL216D	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 Hours of teaching	Total Marks	100
Credits	3	Exam Hours	3
Course Learning Objectives: - To introduce the fundamentals of automotive electronics. - To create complete understanding of Sensors and actuators related to engine. - To study the Digital Control systems of engine. - To impart the knowledge of Bus architectures in automotive field. - To know the Vehicle Electronics Architecture.			
Module-1			
Automotive Fundamentals Overview – Evolution of Automotive Electronics, Automobile Physical Configuration, Survey of Major Automotive Systems, The Engine – Engine Block, Cylinder Head, Four Stroke Cycle, Engine Control, Ignition System – Spark plug, High voltage circuit and distribution, Spark pulse generation, Ignition Timing, Diesel Engine, Drive Train -Transmission, Drive Shaft, Differential, Suspension, Brakes, Steering System Starter Battery -Operating principle: The Basics of Electronic Engine Control – Motivation for Electronic Engine Control – Exhaust Emissions, Fuel Economy, Concept of an Electronic Engine control system, Definition of General terms, Definition of Engine performance terms, Engine mapping, Effect of Air/Fuel ratio, spark timing and EGR on performance, Control Strategy, Electronic Fuel control system, Analysis of intake manifold pressure, Electronic Ignition.			
RBT Levels: L2, L3			
Module-2			
Automotive Sensors – Automotive Control System applications of Sensors and Actuators -Variables to be measured, Airflow rate sensor, Strain Gauge MAP sensor, Engine Crankshaft Angular Position Sensor, Magnetic Reluctance Position Sensor, Hall effect Position Sensor, Shielded Field Sensor, Optical Crankshaft Position Sensor, Throttle Angle Sensor (TAS), Engine Coolant Temperature (ECT) Sensor, Exhaust Gas Oxygen (O ₂ /EGO) Lambda Sensors, Piezoelectric Knock Sensor. Automotive Engine Control Actuators – Solenoid, Fuel Injector, EGR Actuator, Ignition System.			
RBT Levels: L2, L3			
Module-3			
Digital Engine Control Systems -Digital Engine control features, Control modes for fuel Control (Seven Modes), EGR Control, Electronic Ignition Control -Closed loop Ignition timing, Spark Advance Correction Scheme, Integrated Engine Control System- Secondary Air Management, Evaporative Emissions Canister Purge, Automatic System Adjustment, System Diagnostics.			
RBT Levels: L2, L3			
Module-4			
Automotive Networking -Bus Systems – Classification, Applications in the vehicle, Coupling of networks, Examples of networked vehicles Buses – CAN Bus, LIN Bus, MOST Bus, Bluetooth, Flex Ray, Diagnostic Interfaces. Vehicle Motion Control – Typical Cruise Control System, Digital Cruise Control System, Digital Speed Sensor, Throttle Actuator, Digital Cruise Control configuration, Cruise Control Electronics (Digital only), Antilock Brake System (ABS).			
RBT Levels: L2, L3			
Module-5			

Vehicle Electronics Architecture Introduction ,Instrument Cluster ,Heating and Cooling, Airbag Safety Traction and Stability , Power Assist Steering ,Avionics Fly-By-Wire (FBW) ,Automotive X- By-Wire, Tire Pressure Monitoring ,Modules Count , Straight-Wire-Switch Topology , Embedded Function, A Conventional Radio, An Embedded Radio ,Distributed Vehicle Architecture ,Custom Built Modules ,Modules Cross Compatibility , Integrating Dissimilar Functions ,Integrating Identical Functions: A Universal Module, Key-Off Load Current ,12V/42V Electrical Supply System , Vehicle Input Sensors and Switches 1.23 Vehicle Output Devices ,Vehicle Interior Lights Dimming ,H-Bridge Motor Driver ,Microcontrollers Programming Options, Vehicle Operating Softwares.

RBT Levels: L2, L3

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 50% of the maximum marks. Minimum passing marks in SEE is 40% of the maximum marks of SEE. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 50% (50 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

1. Three Unit Tests each of **20 Marks**
2. Two assignments each of **20 Marks** or **one Skill Development Activity of 40 marks**

to attain the COs and POs

The sum of three tests, two assignments/skill Development Activities, will be **scaled down to 50 marks**

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

1. The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 50.
2. The question paper will have ten full questions carrying equal marks.

Suggested Learning Resources:

Books

1. William B. Ribbens, Understanding Automotive Electronics, Seventh edition 2012, Elsevier Publishing.
2. Robert Bosch GmbH (Ed) Bosch Automotive Electrics and Automotive Electronics Systems and Components, Networking and Hybrid Drive, 5th edition, John Wiley & Sons Inc., 2007.
3. Najamuz Zaman" Automotive Electronics Design Fundamentals, Springer International Publishing Switzerland 2015.

Web links and Video Lectures (e-Resources):

1. <https://www.etf.ues.rs.ba/~slubura/Mehatronicki%20sistemi%20kod%20motora%20i%20vozila/Literatura/understanding%20automotive%20electronics.pdf>
2. <https://link.springer.com/book/10.1007/978-3-319-17584-3>

Skill Development Activities Suggested:

1. Interact with industry (small, medium, and large).
2. Involve in research/testing/projects to understand their problems and help creative and innovative methods to solve the problem.
3. Involve in case studies and field visits/ fieldwork.
4. Accustom to the use of standards/codes etc., to narrow the gap between academia and industry.
5. Handle advanced instruments to enhance technical talent.
6. Gain confidence in modelling of systems and algorithms for transient and steady-state operations, thermal study, etc.
7. Work on different software/s (tools) to simulate, analyze and authenticate the output to interpret and conclude.

All activities should enhance student's abilities to employment and/or self-employment opportunities, management skills, Statistical analysis, fiscal expertise, etc. Students and the course instructor/s to involve either

individually or in groups to interact together to enhance the learning and application skills of the study they have undertaken. The students with the help of the course teacher can take up relevant technical –activities which will enhance their skill. The prepared report shall be evaluated for CIE marks.

Course outcome (Course Skill Set)

At the end of the course the student will be able to :

Sl. No.	Description	Blooms Level
C01	Understand fundamentals of automotive electronics.	L2
C02	Apply the Sensors and actuators on engine.	L3
C03	Analyse the Digital Control systems of engine.	L4
C04	Identify the Bus architectures in automotive field.	L1,L2
C05	Gain the knowledge of Vehicle Electronics Architecture	L1,L2

ADVANCED COMMUNICATION LAB			
Course Code	MLELL207	CIE Marks	50
Teaching Hours/Week (L:P:SDA)	1:2:0	SEE Marks	50
Total Hours of Pedagogy	13 Hours of teaching and 10-13 Practical sessions	Total Marks	100
Credits	2	Exam Hours	03
PartA: EDA Using Cadence OrCAD or OrCAD Lite or any EDA Tool,designandverifythefollowing:			
Sl. No.	Experiments		
1	SimulationofASKmodulationanddemodulation		
2	SimulationoffSKmodulationand demodulation		
3	SimulationofBPSKmodulationand demodulation		
4	SimulationofQPSKmodulationand demodulation		
5	SimulationofsignalconstellationQPSKwithRayleighfadingandAWGN		
6	SimulationofsignalconstellationM-aryQAMwith AWGN fading		
7	Tosimulatethecommunicationlink		
8	TosimulateZeroForcingalgorithm		
9	Tosimulate LMSalgorithm		
10	Generationof m-Sequence and verifyits properties		
11	GenerationGold Sequenceand verifyitsproperties		
ConductofPracticalExamination: 1. Alllaboratoryexperiments areto beincludedforpracticalexamination. 2. Studentsareallowed topickoneexperiment fromthelot. 3. Strictlyfollowtheinstructionsasprintedon thecoverpageofanswerscript forbreakup ofmarks. 4. Changeofexperiment is allowedonlyonce and Marksallotted totheprocedureparttobemadezero.			
AssessmentDetails(bothCIEandSEE) TheweightageofContinuousInternalEvaluation(CIE)is50%andforSemesterEndExam(SEE)is50%.Themini- mpassingmarkfortheCIEis 50% of the maximum marks. A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course.The student has to secure not less than 40% of maximum marks in the semester-end examination (SEE). In total of CIE and SEE student has tosecure50% maximum marks ofthe course.			
ContinuousInternalEvaluation(CIE): CIEmarksforthepracticalcourseis 50Marks . Thesplit-upofCIEmarksfor record/journalandtest arein theratio 60:40 . 1. Eachexperimenttobeevaluatedforconductionwithobservationsheetandrecordwrite- up.Rubricsfortheevaluationofthejournal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known tostudentsatthebeginning ofthe practical session. 2. Recordshouldcontainallthespecified experimentsinthesyllabusandeachexperimentwrite- upwillbeevaluated for10marks. 3. Totalmarksscoredbystudentsare scaled downedto30marks(60%ofmaximummarks). 4. Weightageto begivenforneatnessandsubmission ofrecord/write-upontime. 5. Departmentshallconduct02testsfor100marks,thefirsttestshallbeconductedafterthe8 th weekofthese mesterandthesecondtestshall be conducted after the 14 th weekofthe semester. 6. Ineachtest,testwrite-			

up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

7. The suitable rubrics can be designed to evaluate each student's performance and learning ability.
8. The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The sum of **scaled-down** marks scored in the report write-up/journal and average mark of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

9. SEE marks for the practical course is 50 Marks.
10. SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University.
11. All laboratory experiments are to be included for practical examination.
12. (Rubrics) Breakup of marks and the instructions printed on the cover page of the answerscript to be strictly adhered to by the examiners.
OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
13. Students can pick one question (experiment) from the questions not prepared by the internal/external examiners jointly.
14. Evaluation of test write-up/conduction procedure and result/viva will be conducted jointly by examiners.
15. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
16. Change of experiment is allowed only once and 10% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours